An undergraduate laboratory experiment for measuring the energy gap in semiconductors.

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ABSTRACT

A simple and inexpensive apparatus is here described which allows fast and reliable measurements of the temperature dependence of the electrical conductivity in a semiconductor sample. The energy gap can be calculated from the data taken in the intrinsic region, and the temperature dependence of the majority carrier mobility can be deduced from measurements taken in the extrinsic region.

INTRODUCTION

In an introductory course of solid state physics the semiconductors are frequently characterized by the peculiar temperature behavior of their electrical conductivity σ [(1)]. A measurement of σ versus the absolute temperature T, in a sufficiently wide temperature range, may offer a remarkable experimental test of the theoretical predictions of the band model. The apparatus here described does not require expensive instrumentation and it allows precise measurements in a relatively short time interval.

We will assume that the student has been given the basic ideas of the electron-hole pair generation and of the electron scattering processes in solids, and therefore here we will simply recall some relationships that are useful discussing the data collected in the experiment.

The conductivity is defined as the reciprocal of the resistivity $\rho=RA/d$ (where R is the resistance, A the cross-section and d the length of the semiconductor sample), or equivalently as the ratio between the current density $J=I/A$ and the applied electric field $E=V/d$, where I is the current measured when the voltage V is applied across the sample ($\sigma=1/\rho=J/E$).

A doped semiconductor is said to exhibit *extrinsic* behaviour when the dopant concentration N_d is much larger than the concentration of the electron-hole pairs n_i generated by thermal excitations. In this case, provided the temperature is not too low, the "free charge" concentration $n = n_i+N_d \approx N_d$ is temperature independent, and the charge transfer is essentially due to the majority carriers (holes in p-doped , or electrons in n-doped samples). At even lower temperature the semiconductor enters the so called "freeze-out region" and the impurity carrier concentration decreases exponentially as $\exp(-\varepsilon_d/2K_BT)$, where ε_d is the impurity ionization energy ($\varepsilon_d\approx10$ meV in Ge and $\varepsilon_d\approx40$ meV in Si) and K_B is the Boltzmann constant .

In the extrinsic region the current density can be simply written $J=qnv_D=qn\mu E$, where v_D is the drift velocity, μ the mobility and q is the elementary charge. The

electrical conductivity is proportional to the charge carriers concentration and to the mobility : $\sigma=qn\mu$. Therefore in the extrinsic region, since $n\approx$ constant, the temperature dependence of the conductivity and of the mobility are identical. Theoretical calculations [2], accounting for lattice scattering of the charge carriers and neglecting contributions due to scattering with impurities, give a mobility $\mu \propto T^{-\alpha}$, with $\alpha=3/2$. The experimentally observed α value, however, is usually larger than the predicted value 3/2, ranging from 1.6 to 2.5.

The thermal generation of the electron-hole pairs grows exponentially with temperature, and when the temperature is high enough the sample enters the *intrinsic* region where N_d becomes negligible with respect to the concentration of thermally generated electrons (n_i) and holes ($p_i=n_i$). In the intrinsic region we must use the ambipolar conduction formula $\sigma= q(n\mu_n+p\mu_p) = (1+b)\, n_i\mu_n$,where the mobility ratio $b=\mu_n/\mu_p$ is nearly temperature independent [1]. We have $n_i = p_i \propto T^{3/2} \exp[-E_g(T)/2K_BT]$, where $E_g(T)= E_g(0)-\gamma T$ is the temperature dependent [3] energy gap that separates the conduction band from the valence band. Here the temperature dependence of the conductivity is largely dominated by the exponential dependence of the carrier concentration, so that a semilogarithmic plot of σ versus 1/T yields a straight line with slope $E_g(0)/2K_B$.

EXPERIMENTAL APPARATUS

The experiment can be performed using a constant current generator, a voltmeter with high input resistance, a thermometer and a device for changing the sample temperature at a small and constant rate (temperature controller).

We found infact that, for an undergraduate laboratory experiment, it is more practical to take data during a controlled temperature drift than to wait for reaching equilibrium between two consecutive temperature settings. Fast temperature settings can be achieved only using a sophisticated automatic thermoregulator, equipped with a feedback-loop gain controlled by both the error signal and its time derivative[4]. On the other hand the temperature errors introduced by non-equilibrium conditions can be accounted for in the data handling, as explained below.

In our set-up the temperature controller is made by an oven and a simple electronic driving circuit. The oven is obtained from a metallic cylinder (20 mm dia copper tube with a closed end) with a 50 Ω constantan wire heater wound around. The cylinder is suspended inside a glass dewar (figure 1) by means of a stainless steel thin walled tube which carries in six 0.1mm dia copper wires (2 for the heater, 2 for the sample bias current, 2 for the voltage output) and the thermocouple wires. The steel tube provides an effective thermal decoupling from room temperature. Its upper end is soldered to a holder for the electrical connections with measuring apparatus. When the sample temperature must be lowered below 300 K, a copper braid, soldered to the bottom of the oven, provides a good thermal link to a liquid nitrogen (or dry-ice/aceton) bath .

The semiconductor sample is placed inside the oven with the thermocouple junction fastened by PTFE tape. The thermocouple wires should be thin (≈0.15 mm dia) to reduce the temperature error due to conductive thermal coupling. The reference junction must be kept at 0 °C (melting ice bath) : it is convenient to glue it inside a small hole drilled in a metal block, placed into the bath. Alternatively an electronic

"ice point" compensation may be obtained using a diode which senses the room temperature [5].

The Seebeck voltage signal is read on a digital voltmeter (10 MΩ input resistance, 10μV sensitivity), and the temperature is calculated from calibration tables within less than 0.5 °C.

The sample temperature is slowly changed, at a selectable rate, by using the circuit of figure 2a. The heater is driven by a transistor whose working point is voltage-controlled through a simple ramp generator. This is simply an IC integrator with a constant voltage input V_i stabilized by a zener diode. The current charging the capacitor C through the resistor R is kept constant by the feedback loop that holds the inverting input of the operational amplifier to a virtual ground.

Therefore the output voltage is $V_H = -(1/C)\int_0^t (V_i/R)\,dt = -(V_i/RC)\,t$.

With the switch SW1 in PRESET, the initial heating power may be chosen through the potentiometer P_1 which sets the voltage across the integrating capacitor C. With the switch SW1 in RAMP, the positive (SW2 in B) or negative (SW2 in A) slope of the ramp generator is chosen by adjusting the potentiometer P_2. Manual control of the heater is possible in the PRESET configuration.

The resistivity of the sample is measured by the simple circuit of figure 2b. Here a constant current generator provides a selectable and stable current $I=V_Z/R$ across the sample. The sample resistance R_X is calculated from the output voltage as $R_X=V_O/I= R(V_O/V_Z)$. A typical choice is R=2.7kΩ, V_Z=2.7V (I=1mA) for samples with R_X up to 10 kΩ, so that the output reading in volt gives directly the resistance in kΩ. For samples with R_X<1kΩ setting R=270Ω one can stabilize the current up to 10mA.

The semiconductor sample is simply a small bar with appropriate electric contacts. It is important to make the contact resistances r_c negligible with respect to the sample resistance. While it is easy to obtain soldered contacts with low-resistance on germanium samples by using regular acid flux and Sn-Pb soft solder alloy, the same procedure on silicon gives usually rectifying and high-resistance contacts [6]. Good ohmic contacts can be obtained also on Si, by using 50Sn-32Pb-17Cd-1Ag eutectic alloy, if an ultrasonic soldering iron [7] is available. However we found more practical to use as Si sample an unijunction transistor, taking advantage of the fact that this device has the base pins B1 and B2 connected with ohmic contacts to the semiconductor substrate. The emitter pin E, which is connected to the p-n junction, for our purpose is disregarded.

If very low resistance samples are used (R_X<100Ω), the systematic errors due to the voltage drop across the current carrying wires and to the contact resistances may be not negligible. In this case a four-wires circuit as that shown in figure 2c should be used. Here two separate contact pairs are made at both sample ends : one (AB) for current feed and one (CD) for voltage detection. With this set-up, the potential difference V_D-V_C equals the true voltage drop across the crystal if the measuring instrument sinks a negligible current. The differential amplifier of figure 2c should be made with FET-input operational amplifiers (input current < 1nA), or it may be replaced by a high impedance (≈100MΩ) floating input voltmeter.

THE EXPERIMENT

A typical run is performed within less than 2 hours, with the temperature changing at a rate $\partial T/\partial t \approx 5\times10^{-2}$ Ks^{-1}. Using a liquid nitrogen bath the temperature can be varied in the range 80 K<T<430 K, and with dry ice melting in aceton bath the lower limit

is ≈200 K. The upper limit is imposed by the melting of the Sn-Pb solder contacts on the germanium sample. If a unijunction transistor is used as sample, one can reach an upper temperature T≈520 K.

It is convenient to use *slightly* doped semiconductor samples [8], if both the energy gap and the mobility behaviour with temperature has to be measured . In *heavily* doped samples infact the extrinsic region extends up to high temperatures, and to observe the intrinsic behaviour one has to work above 200 °C , where the soft soldered contacts melt . See for example the technique used by Fox and Gaggini[9].

The smaller is the temperature slope $\partial T/\partial t$, the smaller are the thermal gradients $\partial T/\partial x$. An evaluation of (and a correction for) the errors due to gradients can be obtained by measuring the resistance at the same observed T values both increasing and decreasing the temperature : the average between these two values cancels the systematic error if the slope $|\partial T/\partial t|$ is the same.

The experimental results obtained in two typical runs are shown in figure 3, for a germanium sample (n-doped, $\rho \approx 14\ \Omega$ cm) and for an unijunction transistor Texas 2N2160 (metal case), respectively. Here T is the temperature in Kelvin and t (=273.15+T) is the temperature in Celsius.

Figure 4a shows the Ge resistance in the intrinsic region plotted versus the reciprocal absolute temperature 1/T in a semilog plot. The slope of the linear fit for 58°C <t<143°C gives $E_g(0)=0.79\pm 0.02$ eV. The same plot for the Si sample is shown in figure 4b. The best fit in the temperature range 185°C <t<255°C gives $E_g(0)=1.18\pm 0.02$eV.

In figure 4c the $\log_{10}R$ for the germanium sample is plotted versus $\log_{10}T$ and the slope of the fitting line for -160°C <t<-10°C gives $\alpha=1.65\pm0.02$. The extrinsic region for the unijunction transistor (figure 4d) spans the temperature range -100°C <t< +100°C and the exponent in the power law $\mu \propto T^{-\alpha}$ is $\alpha=2.30\pm 0.03$. The slight deviation from linearity at the lowest temperatures indicates the beginning of the "freeze-out region".

These results can be compared with the rather scattered α–values given in the literature [10] [$\alpha=1.6\div1.7$ for electrons in Ge, $\alpha=2.3\div2.6$ for electrons in Si], and with the commonly quoted values [3] for the energy gap linearly extrapolated to 0 K [$E_g(0)=0.782$ ev in Ge and $E_g(0)=1.205$ eV in Si] .

REFERENCES

(1) Two useful texts which give exhaustive treatments of this subject are J.P.McKelvey , *Solid State and Semiconductor Physics*, New York, Harper &Row (1966) and R.A.Smith, *Semiconductor*, New York,Cambridge Univ. Press (1981)
(2) See for example W.Shockley, *Electrons and Holes in Semiconductors*, New York,D.van Nostrand (1950) and the more recent J.S.Blakemore *Solid State Physics*, Cambridge,Cambridge Univ.Press (1985) p.306.
(3) C.Kittel, *Introduction to Solid State Physics*, New York,Wiley (1968). The temperature dependence of the energy gap was measured by optical absorption by G.G.Macfarlaine et al., Phys.Rev.108,1377(1957) and 111,1245(1958). Above 200 K the results are well described by E_g=(0.782-0.0004 T) eV for Ge, and by E_g=(1.205-0.0003 T) eV for Si.
(4) L.Bruschi, R.Storti and G.Torzo, Rev. Sci. Instrum., 56,427(1985)
(5) See for example : AD590 Application Note, INTERSIL Catalog, 5-1 (1986), and LM134 Application Note, NATIONAL Linear Data Book, 9-17 (1982)
(6) A.Sconza and G.Torzo Eur.J.Phys.8,34(1987); A.Sconza and G.Torzo Eur.J.Phys.6,295(1985).
(7) We used model G35/T35 soldering iron and type S-100-a-11 solder, manufactured by FIBRASONIC Inc.,Chicago, Illinois.
(8) The dopant concentration has to be compared with the intrinsic carrier concentration n_i : at room temperature for pure Si we have $n_i \approx 10^{10}$ cm^{-3} ($\rho \approx 2.6 \times 10^5$ Ω cm) and for pure Ge $n_i \approx 10^{13}$ cm^{-3} ($\rho \approx 43$ Ω cm) .
(9)J.N.Fox and N.W.Gaggini, Eur.J.Phys.8,273(1987). It must be noted that the energy gap value 1.15 eV, quoted by these authors as expexted value for Si, is not the value linearly extrapolated toT=0 K but the one measured at T≈0 K: see references 2 and 3.
(10) See for example J.M.Ziman *Electrons and Phonons*, Oxford, Clarendon Press (1960) p. 443 and A.Alberigi Quaranta, M.Martini and G.Ottaviani in *Semiconductor Detectors* , G.Bertolini and A.Coche Editors, North Holland (1968) p.61, and references therein. It must be noted that the measured α value is due to the contribution of various scattering mechanisms. Lattice scattering is dominant in pure and perfect crystals, while impurity scattering and dislocation scattering may become important in less perfect samples. Moreover α depends on the mearuring method , i.e. conductivity (as in our work) or drift time, or Hall mobility.

FIGURE CAPTIONS

Figure 1 : A schematic draw of the experimental apparatus

Figure 2 : The electronic circuitry : (a) heater driver , (b) constant current generator , (c) 4-wires configuration to avoid the effect of contact resistances

Figure 3 : The voltage drop measured across the semiconductor samples in the whole temperature range. The Germanium sample is a 2x2x10 mm bar, n-doped. The Silicon sample is the base, n-doped, of a 2N2160 unijunction transistor

Figure 4 : (a) and (b): the linear fit in the intrinsic region (high temperature); (c) and (d): linear fit in the extrinsic region (low temperature)

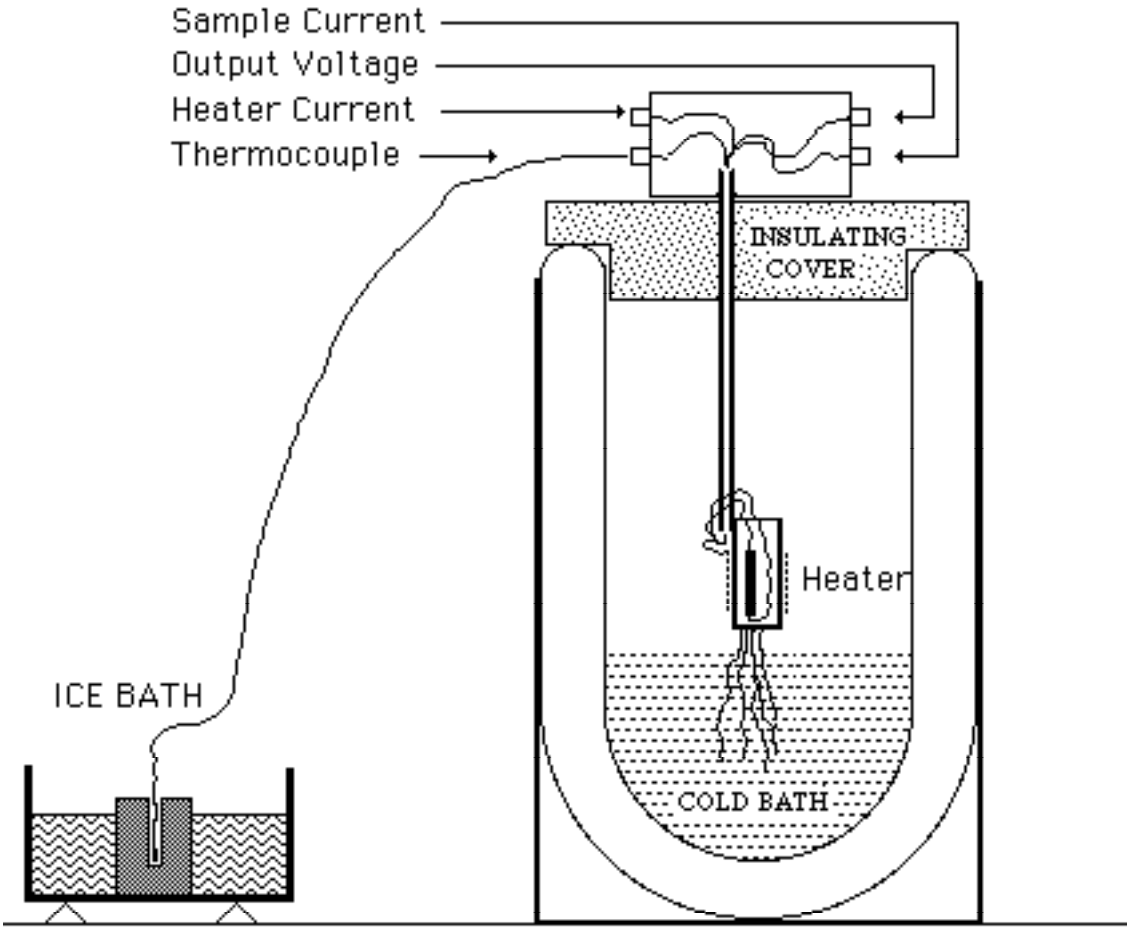
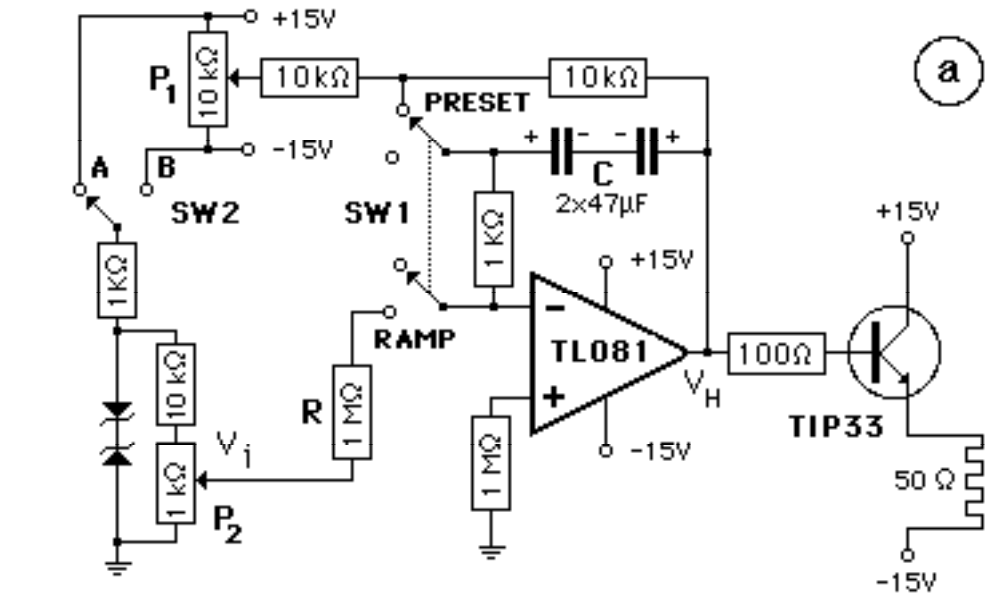
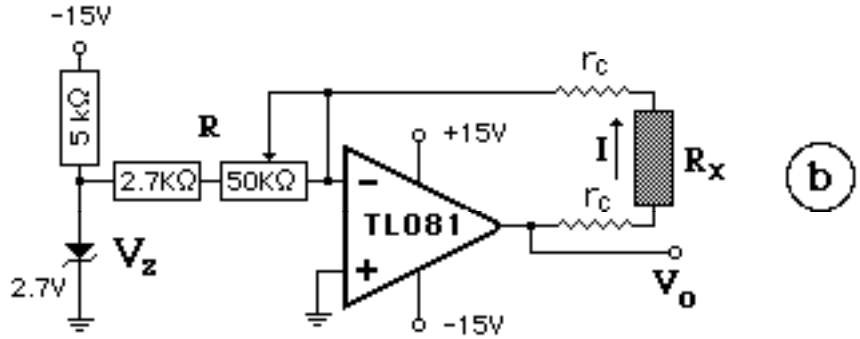

Sample Current
Output Voltage
Heater Current
Thermocouple
INSULATING COVER
Heater
ICE BATH
COLD BATH

Figure 1


+15V
P1
10 kΩ
10kΩ
10kΩ
PRESET
a
-15V
A
B
SW2
SW1
C
2x47µF
1 KΩ
+15V
1KΩ
+15V
RAMP
TL081
100Ω
10 kΩ
R
1 MΩ
VH
TIP33
Vi
1 kΩ
P2
1 MΩ
-15V
50 Ω
-15V


-15V
5 kΩ
rc
R
+15V
I
Rx
2.7KΩ
50KΩ
TL081
b
rc
Vz
2.7V
Vo
-15V

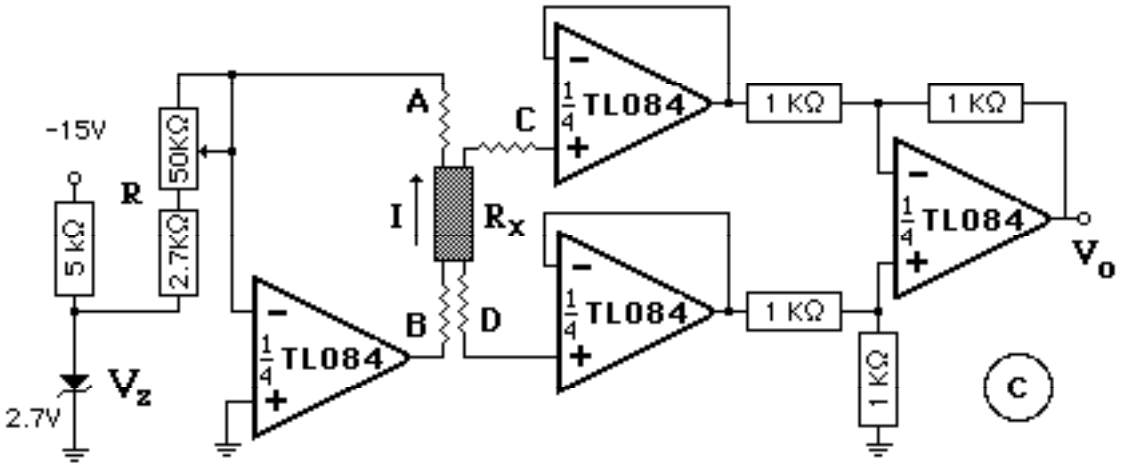

A
C
-15V
50KΩ
1/4 TL084
1 KΩ
1 KΩ
R
I
Rx
1/4 TL084
Vo
5 kΩ
2.7KΩ
B
D
1/4 TL084
1 KΩ
Vz
1 KΩ
c
2.7V

Figure 2

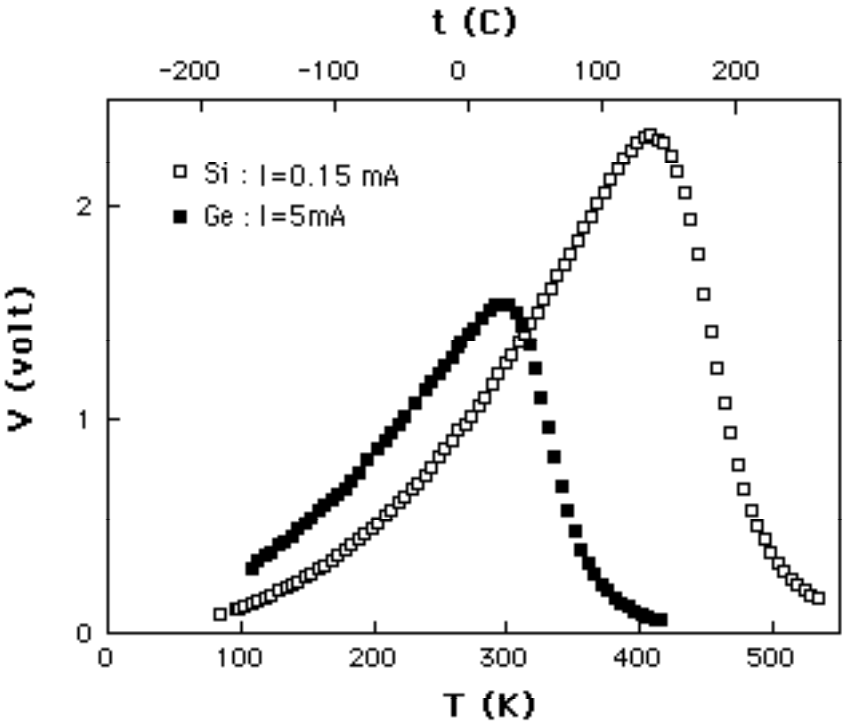

t (C)
-200
-100
0
100
200
Si : I=0.15 mA
Ge : I=5mA
V (volt)
0
1
2
0
100
200
300
400
500
T (K)

Figure 3

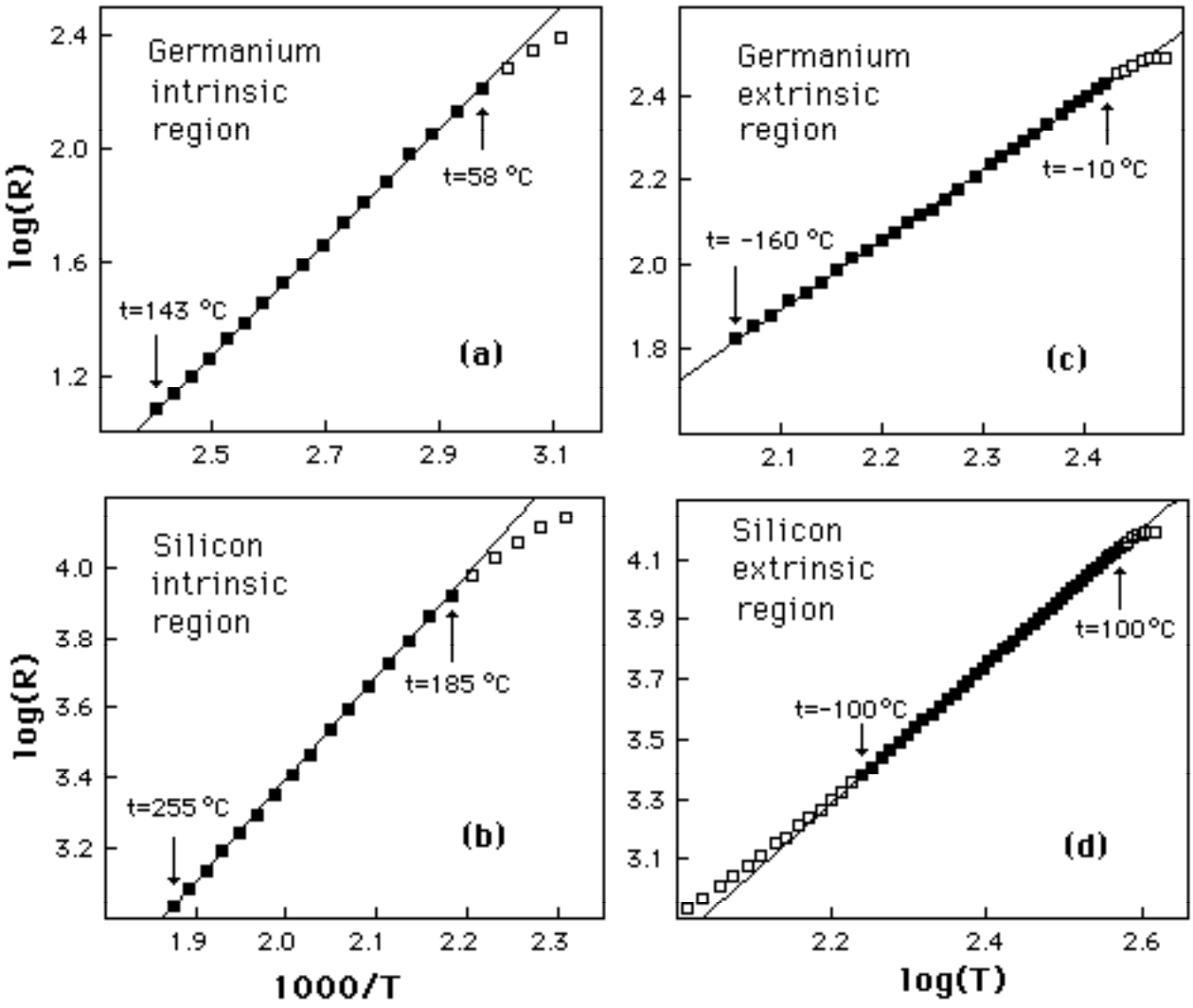

Germanium
intrinsic
region
t=58 °C
t=143 °C
(a)
log(R)
Germanium
extrinsic
region
t= -10 °C
t= -160 °C
(c)
Silicon
intrinsic
region
t=185 °C
t=255 °C
(b)
1000/T
Silicon
extrinsic
region
t=100°C
t=-100°C
(d)
log(T)

Figure 4